EXAMINER'S AMENDMENT

1. Claims 1-5, 7-15, 17-20, 26, 28-31, 33, 34, and 36 are pending in the instant application.

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Arlene Neal on April 14, 2008.

The application has been amended as follows wherein the following versions of claims 1, 7-11, 13, 17-20, 26, 28-31, 33, 34, and 36 replace all prior versions in their entirety:

1. A method comprising:

receiving from a transmitter, by a receiver, a transmitted phase difference information indicating a phase difference between an internal clock and an external clock of the transmitter;

generating, by the receiver, a clock signal dependent on the ~~transmitted~~ phase difference information

generating, by the receiver, ~~an~~ a receiver internal clock ~~or~~ by recovering ~~an~~ the internal clock of ~~a~~ the transmitter from information received from the transmitter;

frequency-dividing, by the receiver, the receiver internal clock;

storing, by the receiver, at least two successive values of the phase difference information received from the transmitter;

detecting, by the receiver, a difference between the at least two successive values of phase difference information; and

adjusting, by the receiver, the phase of the frequency-divided clock based on the detected difference.

7. The method according to claim 1, further comprising multiplying, by the receiver, the frequency of the adjusted frequency-divided clock for generating ~~an~~ a frequency multiplied receiver external clock.

8. The method according to claim 7, wherein a receiver external clock is generated from the phase adjusted frequency-divided clock by ~~comprising including, by the receiver, a clock generator stage for generating the external clock, the clock generator stage comprises a first counter for~~ first counting, in a round-rotating manner, a high frequency signal, and ~~a second counter for~~ second counting the number of rounds of the first counting ~~counter~~, the second ~~counter~~ counting inhibiting the first ~~counter~~ counting from further counting when reaching a preset value.

9. The method according to claim 1, comprising:

selecting, by the receiver, depending on the difference between the at least two successive values of phase difference information, one of the stored values of the phase difference information for adjusting the phase of the frequency-divided clock.

10. The method according to claim 1, comprising:

suppressing, by the receiver, depending on the difference between the at least two successive values of the phase difference information, generation of a second pulse within one period of the frequency-divided clock.

11. A system comprising:

a transmitter comprising a phase difference information generator configured to generate phase difference information indicating a phase difference between an internal clock and an external clock, and a ~~transmittor~~ transmitter configured to transmit the phase difference information to ~~the~~ a receiver; and

~~a~~ the receiver comprising a phase receiver configured to receive ~~a~~ the phase difference information indicating ~~a~~ the phase difference between ~~an~~ the internal clock and ~~an~~ the external clock, a clock generator configured to generate a clock signal dependent on the transmitted phase difference information, a generator configured to generate ~~an~~ a receiver internal clock ~~or~~ by recovering ~~recover~~ the internal clock of the transmitter from information received from the transmitter, a frequency-divider configured to frequency-divide the receiver internal clock, a storage configured to store at least two successive values of the phase difference information received from the transmitter, a detector configured to detect a difference between the at least

two successive values of phase difference information and an adjuster configured to adjust the phase of the frequency-divided clock based on the detected ~~phase~~ difference.

13. The system according to claim 12, wherein the converter comprises a counter which generates the numerical value to be transmitted to the receiver, the counter having start and stop inputs to which pulses of the frequency-divided clocks are ~~applicable~~ applied.

17. The system according to claim 11, wherein the receiver further comprises a multiplier configured to multiply the frequency of the adjusted frequency-divided clock for generating ~~an~~ a frequency multiplied receiver external clock.

18. The system according to claim 17, wherein the receiver further comprises a clock generator stage configured to generate ~~an~~ a receiver external clock from the phase adjusted frequency-divided clock, wherein the clock generator stage comprises a first counter for counting, in a round-rotating manner, a high frequency signal, and a second counter for counting the number of rounds of the first counter, the second counter inhibiting the first counter from further counting when the first counter reaches a preset value.

19. The system according to claim 11, wherein the receiver further comprises:

a selector configured to select, depending on the difference between the at least two successive values of the phase difference information, one of the stored values of the phase difference information for adjusting the phase of the frequency-divided clock.

20. The system according to claim 11, wherein the receiver further comprises:

a suppressor configured to suppress, depending on the difference between the at least two successive values of the phase difference information, generation of a second pulse within one period of the frequency-divided clock.

26. An apparatus comprising:

a receiver configured to receive, from a transmitter, ~~a~~ transmitted phase difference information indicating a phase difference between an internal clock and an external clock of the transmitter;

a clock generator configured to generate a clock signal dependent on ~~a~~ the phase difference information transmitted from ~~a~~ the transmitter;

a generator configured to generate ~~an~~ a receiver internal clock~~, or to recover~~ by recovering the internal clock of the transmitter from information received from the transmitter;

a frequency-divider configured to frequency-divide the receiver internal clock;

storages for storing at least two successive values of the phase difference information received from the transmitter;

a detector configured to detect a difference between the at least two successive values of the phase difference information; and

an adjuster configured to adjust the phase of the frequency-divided clock based on the detected difference.

28. The apparatus according to claim 26, further comprising a multiplier configured to multiply ~~the~~ a frequency of a receiver external clock ~~the adjusted frequency-divided clock~~ for generating ~~an~~ a frequency multiplied receiver external clock.

29. The apparatus according to claim 26, further comprising a clock generator stage configured to generate ~~an~~ a receiver external clock from the phase adjusted frequency-divided clock, the clock generator stage ~~comprises~~ comprising a first counter for counting, in a round-rotating manner, a high frequency signal, and a second counter for counting the number of rounds of the first counter, the second counter ~~inhibits~~ inhibiting the first counter from further counting when the first counter reaches a preset value.

30. The apparatus according to claim 26, comprising:

a selector configured to select, depending on the difference between the at least two successive values of the phase difference information, one of the stored values of the phase difference information for adjusting the phase of the frequency-divided clock.

31. The receiver according to claim 26, comprising:

a suppressor configured to suppress, depending on the difference between the at least two successive values of the phase difference information, generation of a second pulse within one period of the frequency-divided clock.

33. A method, comprising:

receiving from a transmitter, by a receiver, ~~a~~ transmitted phase difference information indicating a phase difference between an internal clock and an external clock of the transmitter;

generating, by the receiver, a clock signal dependent on a received phase difference information indicating a phase difference between the internal and the external clock of the transmitter, the phase difference information being received from the transmitter;

generating, by the receiver, ~~an~~ a receiver internal clock ~~or~~ by recovering the internal clock of the transmitter from information received from the transmitter;

frequency-dividing, by the receiver, the receiver internal clock;

storing, by the receiver, at least two successive values of the phase difference information received from the transmitter;

detecting, by the receiver, a difference between the at least two successive values of phase difference information; and

adjusting, by the receiver, the phase of the frequency-divided clock based on the detected difference.

34. A system comprising:

a transmitter comprising a phase difference information generating means for generating phase difference information indicating a phase difference between an internal clock and an external clock, and transmitting means for transmitting the phase difference information to ~~the~~ a receiver; and

~~a~~ the receiver comprising a receiving means for receiving ~~a~~ the phase difference information indicating a phase difference between ~~an~~ the internal clock and ~~an~~ the external clock, a clock generator means for generating a clock signal dependent on the ~~transmitted~~ phase difference information, generating means for generating ~~an~~ a receiver internal clock ~~or~~ by recovering the internal clock of the transmitter from information received from the transmitter, frequency-dividing means for frequency dividing the receiver internal clock, storing means for storing at least two successive values of the phase difference information received from the transmitter, detecting means for detecting a difference between the at least two successive values of phase difference information and adjusting means for adjusting the phase of the frequency-divided clock based on the detected difference.

36. An apparatus, comprising:

a receiving means for receiving, from a transmitter, a phase difference information indicating a phase difference between an internal clock and an external clock;

a clock generator means for generating a clock signal dependent on the ~~transmitted~~ phase difference information;

generating means for generating ~~an~~ a receiver internal clock ~~or~~ by recovering the internal clock of the transmitter from information received from the transmitter;

frequency-dividing means for frequency dividing the receiver internal clock;

storing means for storing at least two successive values of the phase difference information received from the transmitter;

detecting means for detecting a difference between the at least two successive values of phase difference information; and

adjusting means for adjusting the phase of the frequency-divided clock based on the detected difference.

Claims 1-5, 7-15, 17-20, 26, 28-31, 33, 34, and 36 are renumbered respectively as claims 1-26, and the claim dependency is renumbered accordingly.

Allowable Subject Matter

3. Claims 1-5, 7-15, 17-20, 26, 28-31, 33, 34, and 36 renumbered respectively as claims 1-26 are allowed.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON M. PERILLA whose telephone number is (571)272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jason M. Perilla/
April 15, 2008

/jmp/

/Chieh M Fan/
Supervisory Patent Examiner, Art Unit 2611